

FIGURE 2

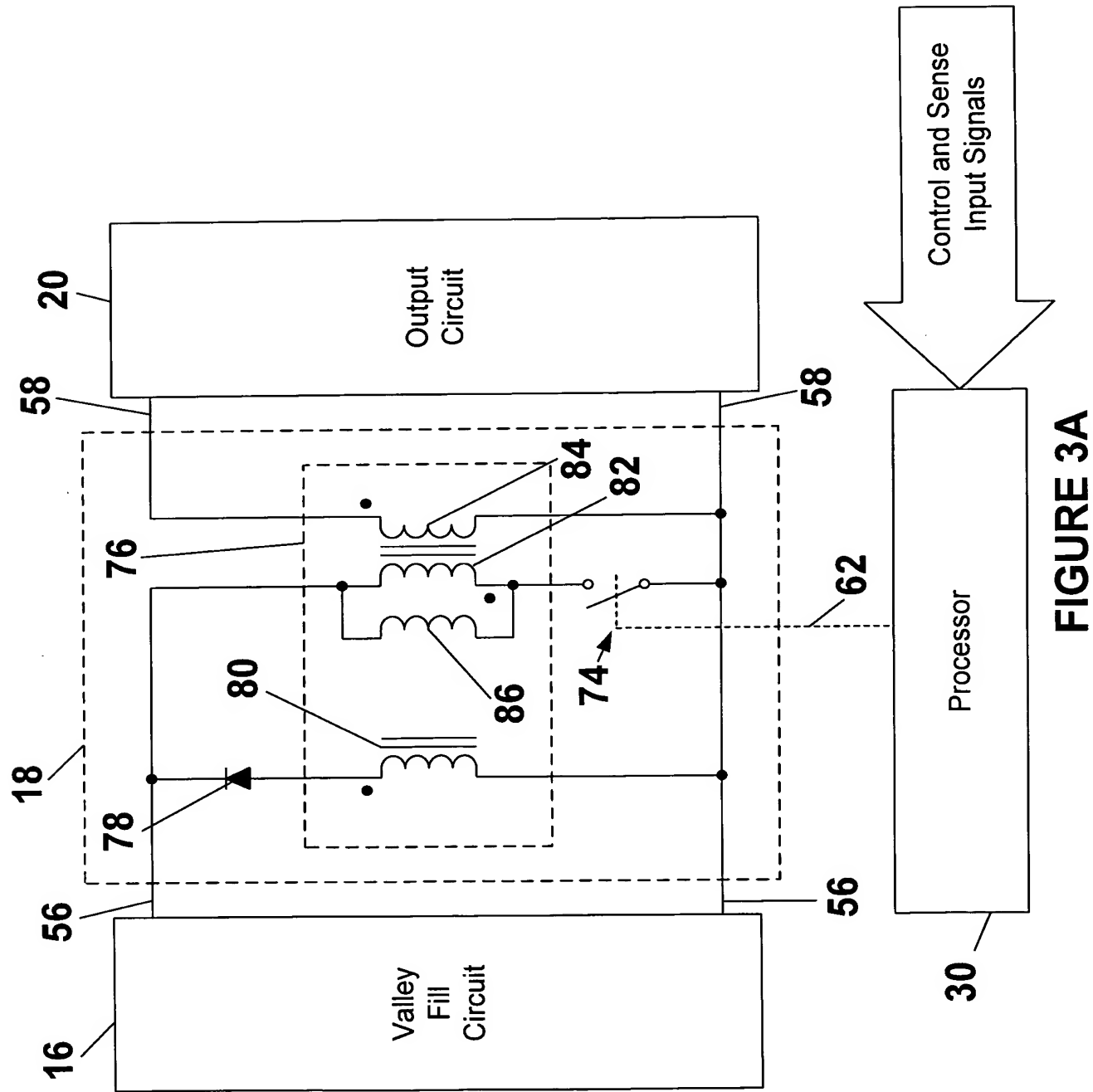


FIGURE 3A

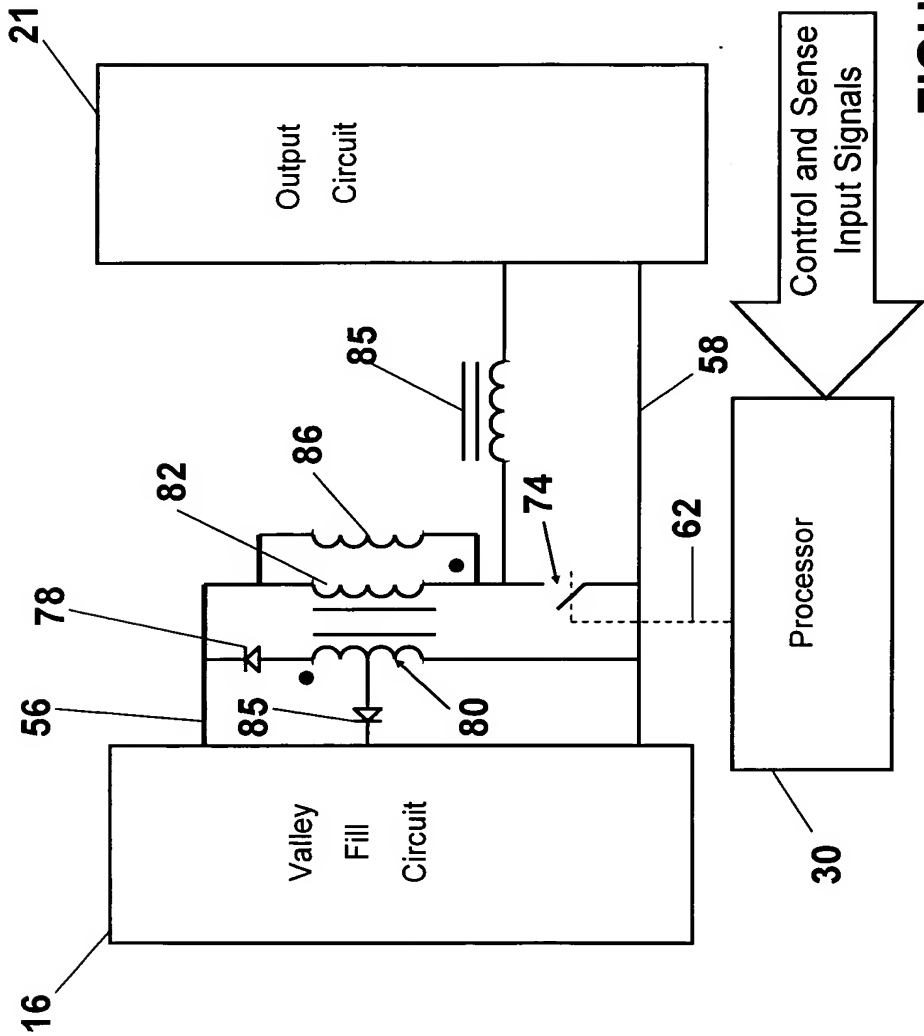


FIGURE 3B

PROCESSOR CONTROLLED BALLAST STATES

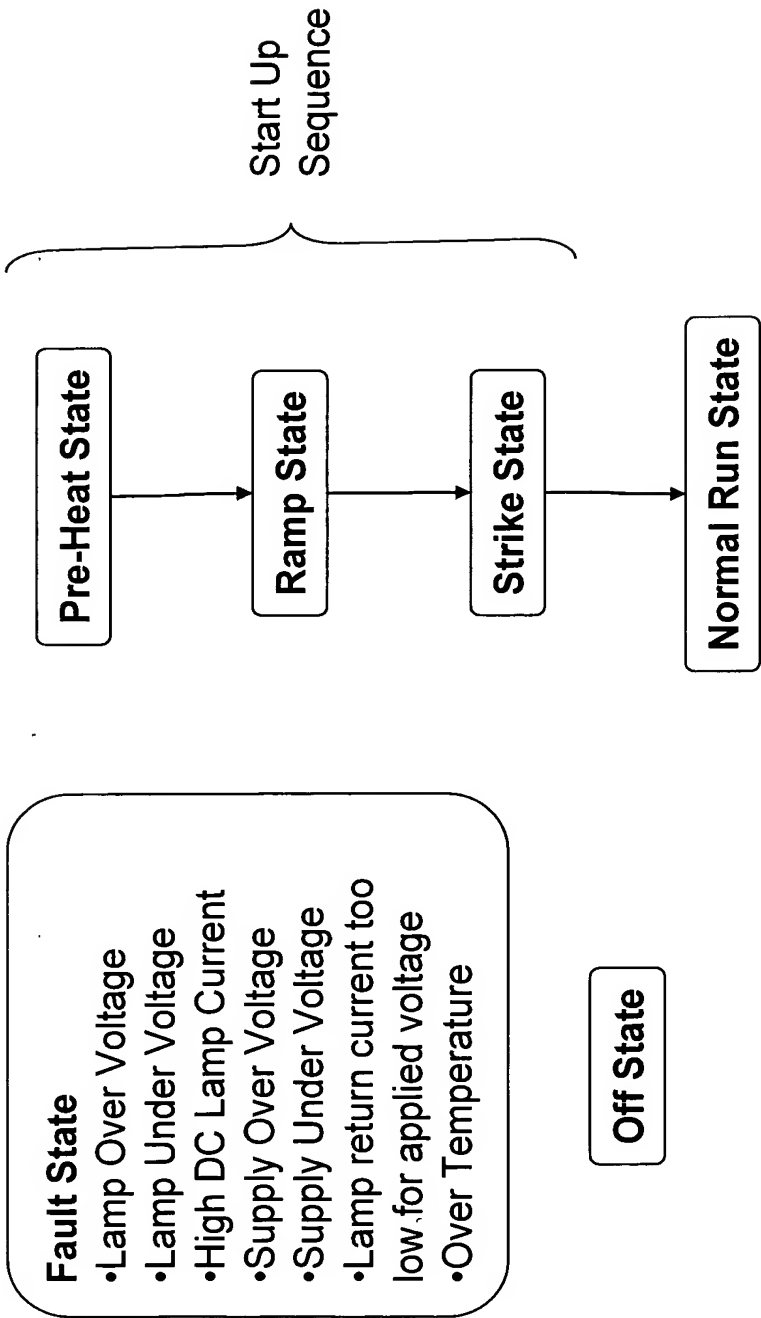


FIGURE 4

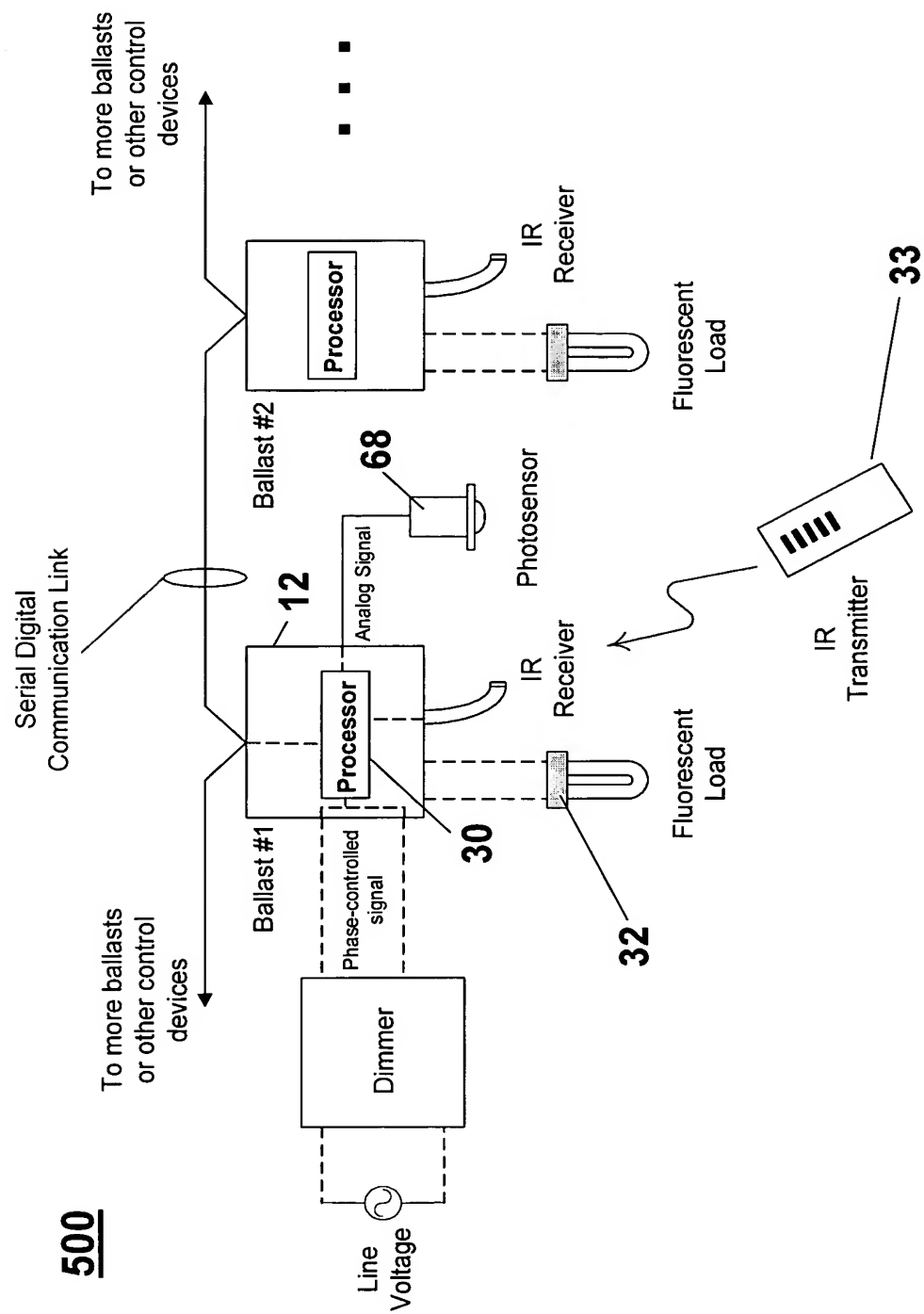


FIGURE 5

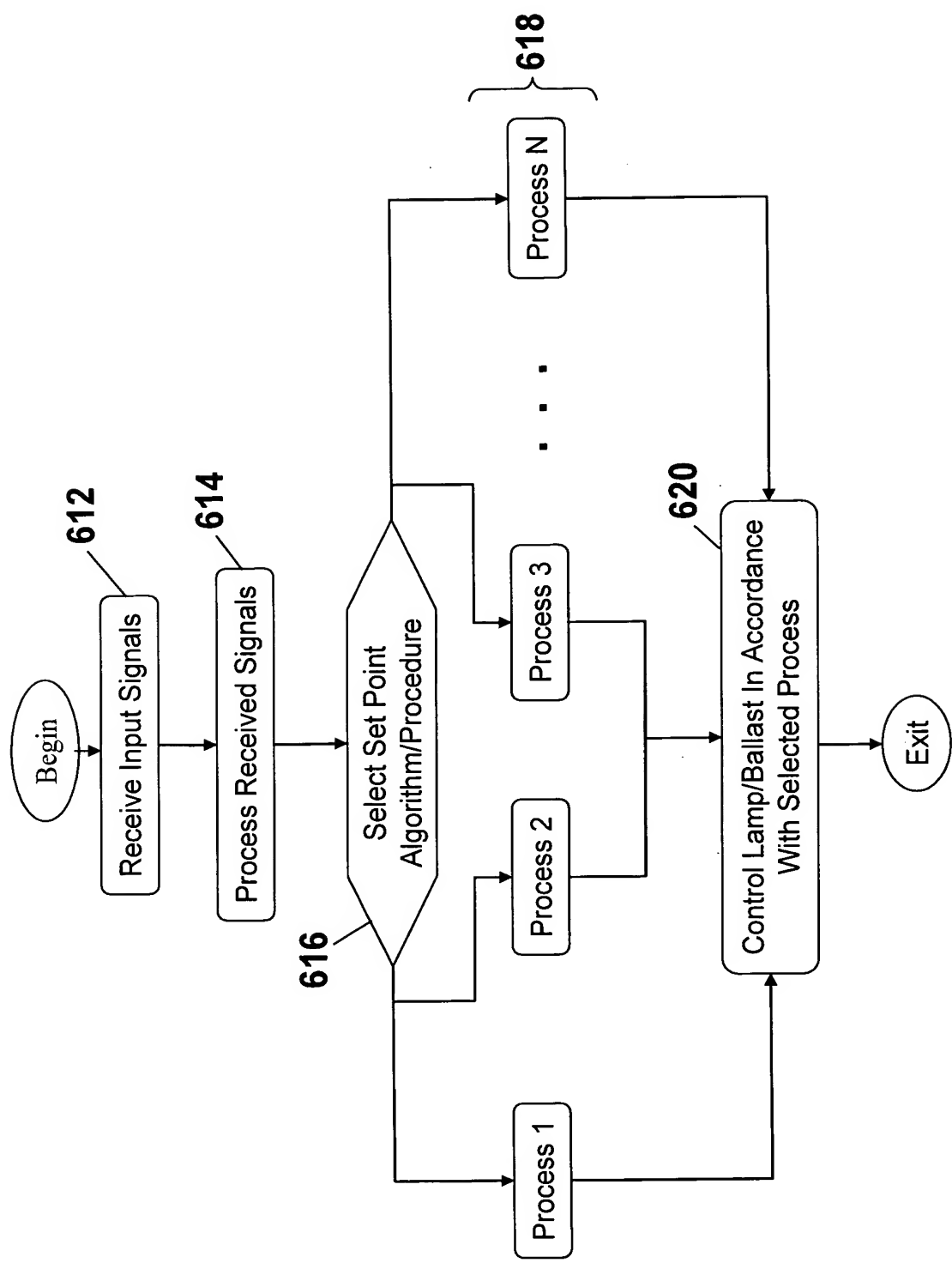


FIGURE 6

700

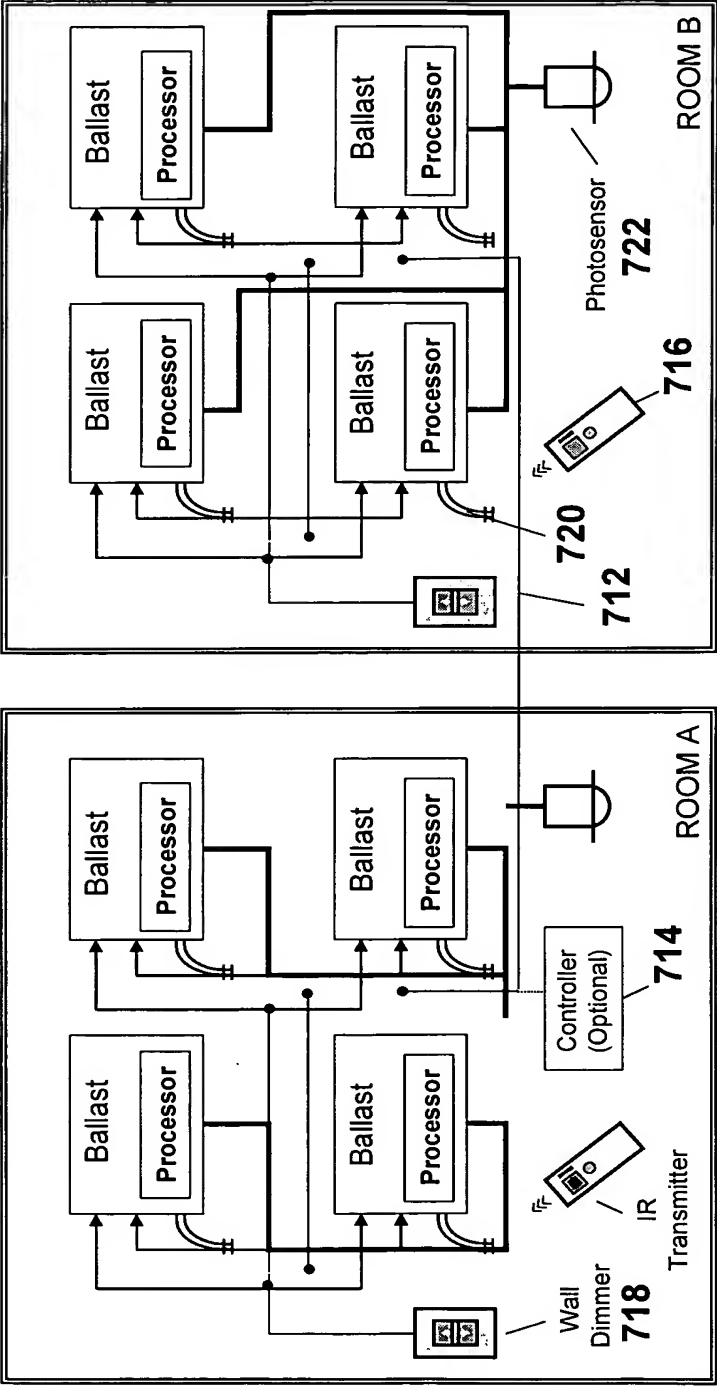


FIGURE 7

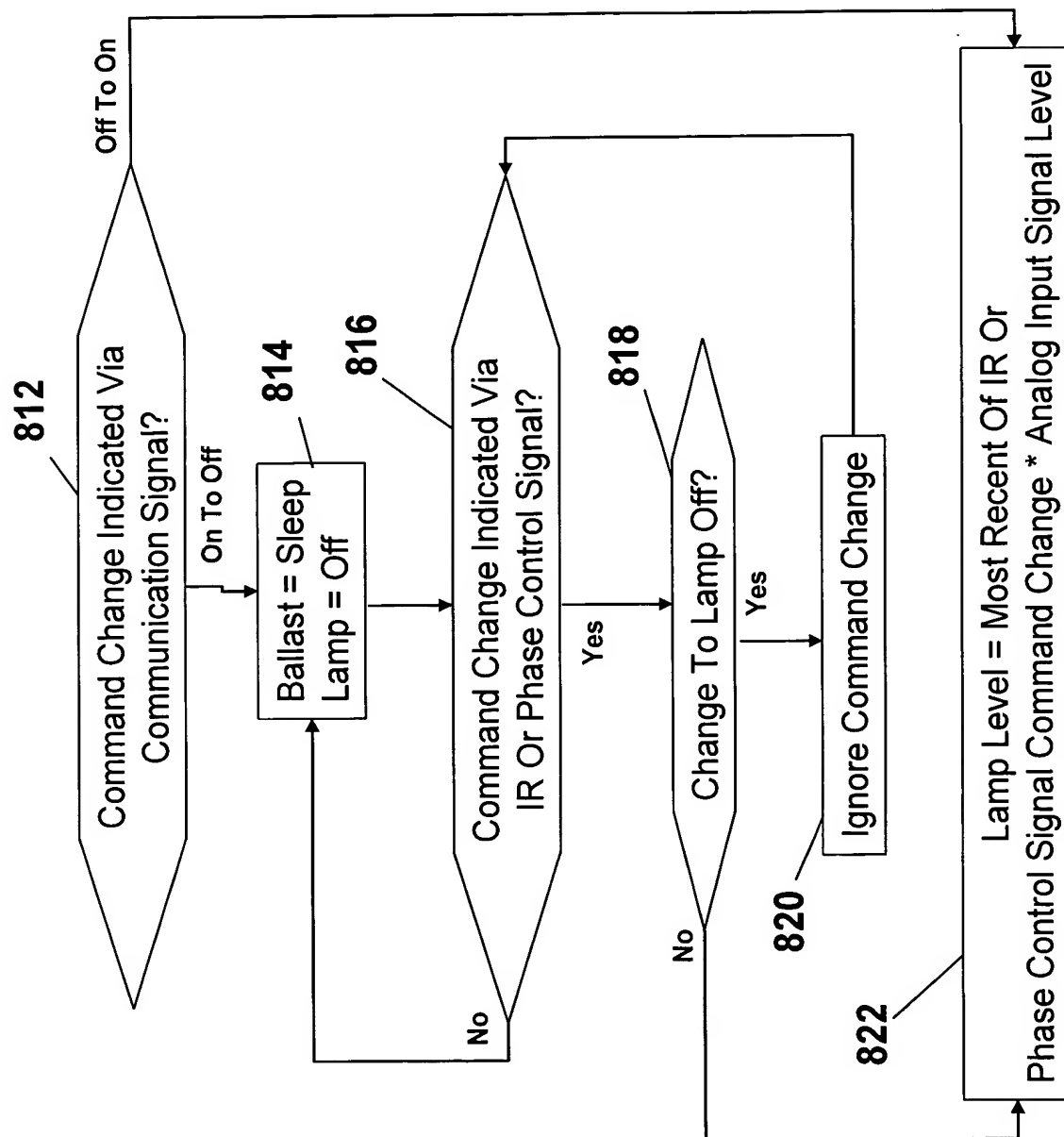
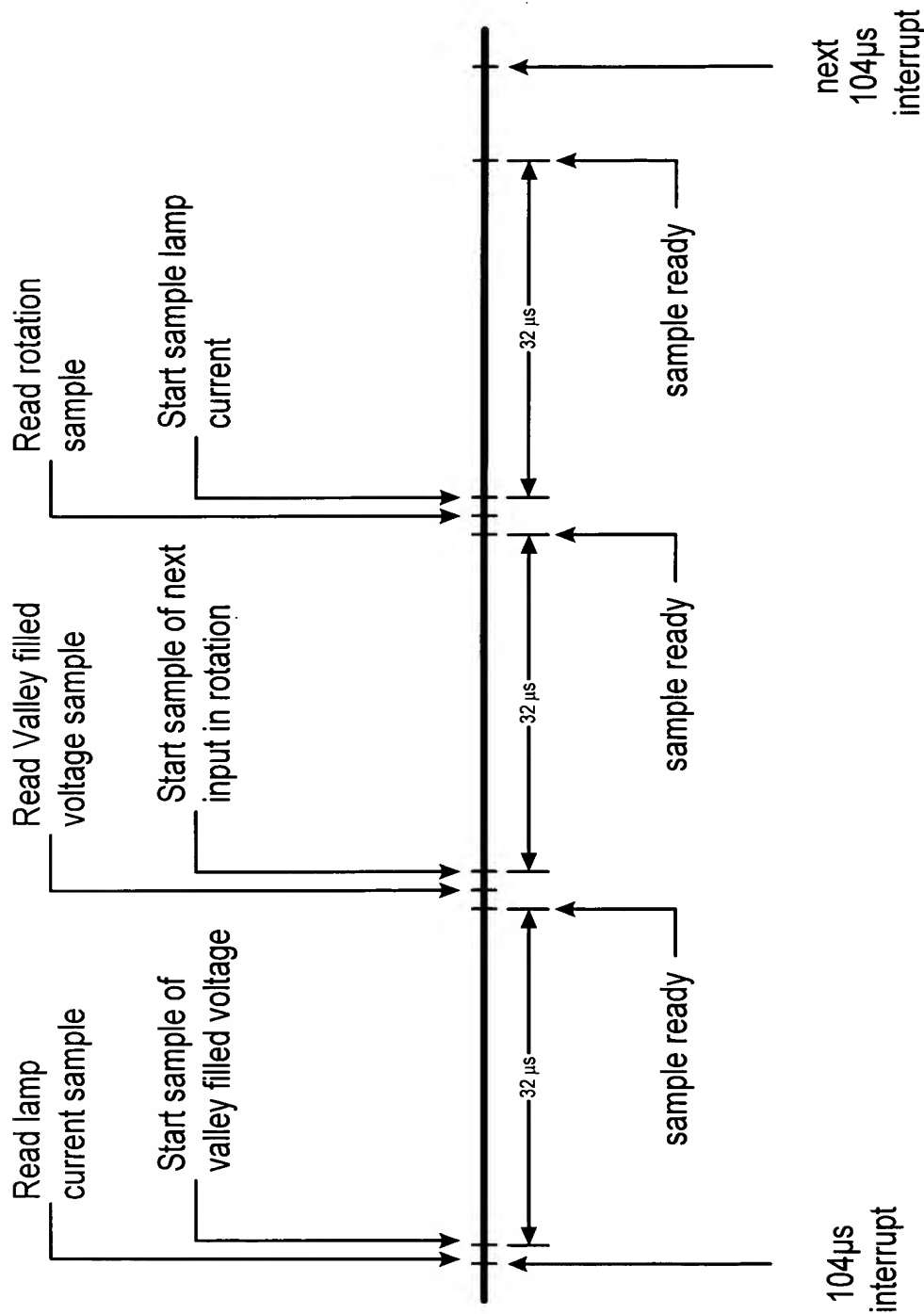


FIGURE 8



next
104 μs
interrupt

FIGURE 9

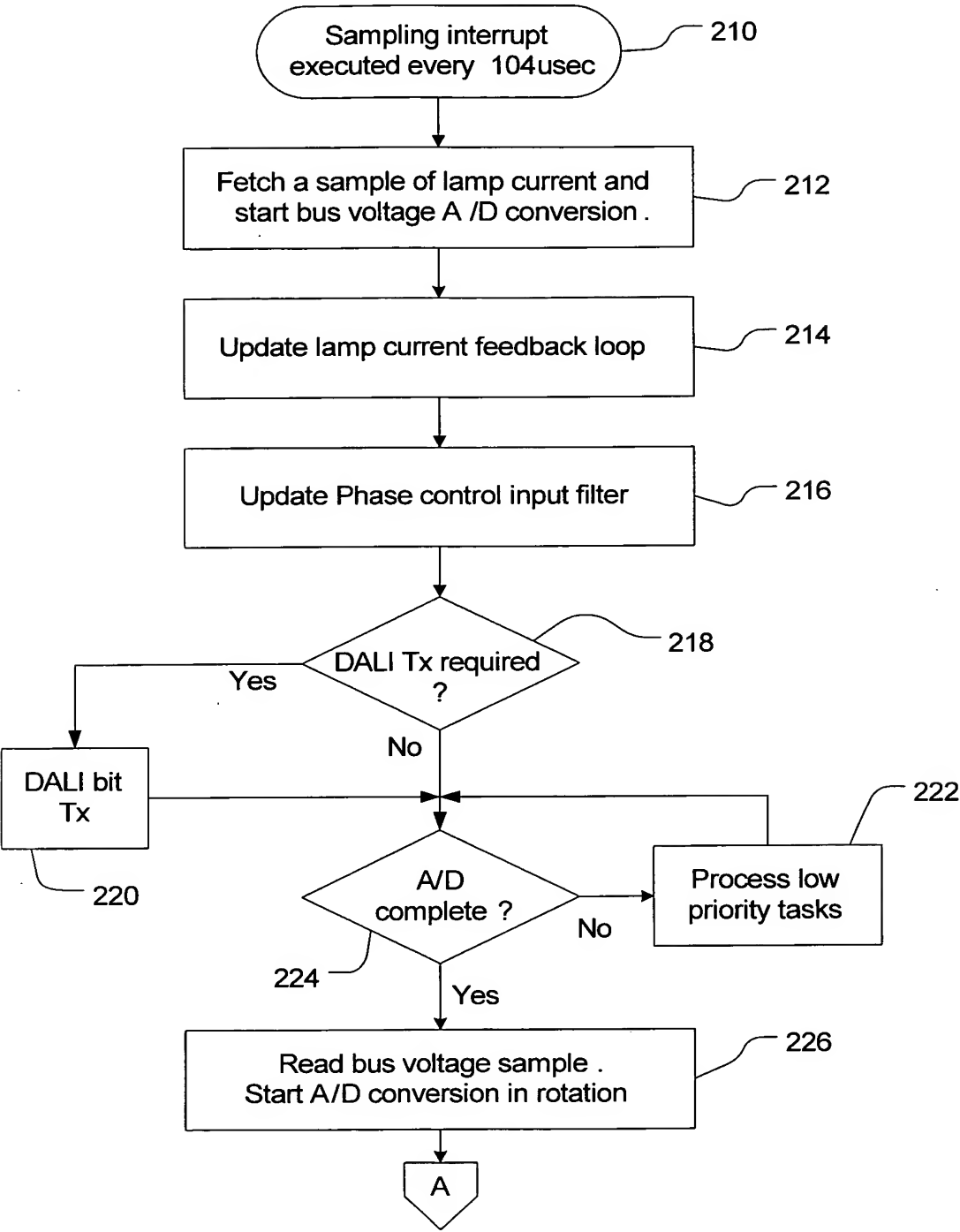


FIGURE 10A

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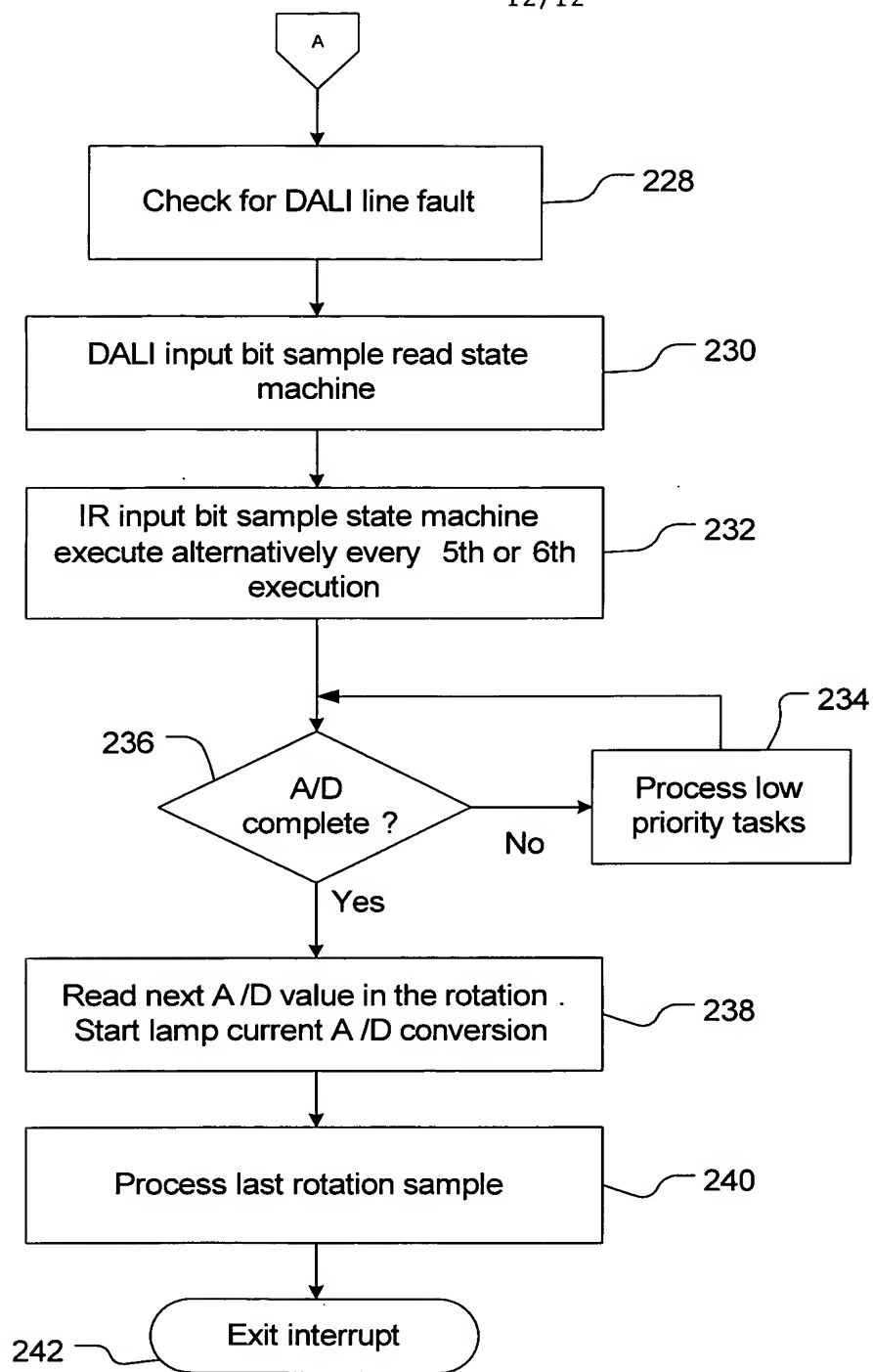


FIGURE 10B